## REMARKS

In section 3 of the Office Action, the Examiner objects to the title of the invention as being not descriptive. The title has been amended to "fuse structure used in an integrated circuit device". The Applicants believe that the new title is descriptive and that the objection to the title has been overcome.

In section 4, the Examiner objects to claim 22, suggesting deleting "Each" and insert "each". Claim 22 has been amended accordingly.

In section 5, the Examiner rejects claims 1-26 under 35 USC 112, second paragraph. In particular, the Examiner asserts that the limitation "an optimal position of laser spot defined above a substrate" is not clear. Such phrase has been amended to "a substrate" in claims 1, 9, 15 and 22. The Applicants believe that such rejection has been overcome.

Furthermore, the phrase "the laterals of the second conductive layer" in claim 9 has been amended to "both sides of the second conductive layer". In claim 22, the phrase "wherein each fuse structure has its own the position of laser spot on the second conductive layer" has been amended to "wherein each fuse structure has one position of laser spot on the second conductive layer". The objected phrase at lines 15-19 of claim 22 has been removed. The Applicants believe that the rejections under 35 USC 112, second paragraph have been overcome.

In section 6, the Examiner rejects claims 1-6, 9-19 and 22-26 under 35 USC 102(b) as being anticipated by Kokubun (US Patent No. 6,008,716). Moreover, in section 7, claims 1-4, 6, 15-17, 19 and 20 are rejected under 35 USC 102(b) as being anticipated by Niwa (US Patent No. 6,218,721). In section 8, claims 15, 18, 20, 22 and 25 are rejected under 35 USC 102(a) as being anticipated by AAPA. In section 9, claims 5, 18 and 21 are rejected under 35 USC 103(a) as being unpatentable over Niwa. These rejections are respectfully traversed.

Kokubun, Niwa, and AAPA, standing alone or in combination, fails to disclose, teach, or suggest, *inter alia*, the following features recited by the claimed invention:

Claim 1: "a third conductive layer formed on the part of the dielectric layer placed above the first conductive layer and corresponding to the first conductive layer, wherein the third conductive layer is insulated from the first and second conductive layers, and the second conductive layer and the third conductive layer are arranged in a straight line";

Claim 9: "a third conductive layer formed on the part of the dielectric layer placed above the first conductive layer and corresponding to the first conductive layer, wherein the third conductive layer is insulated from the first and second conductive layers, and the second conductive layer and the third conductive layer are arranged in a straight line";

Claim 15: "a second conductive layer comprising a position of laser spot formed on the dielectric layer, wherein a portion of the second conductive layer not having the position of laser spot corresponds to the first conductive layer";

Claim 22: "a second conductive layer comprising a position of laser

spot formed on part of the dielectric layer, wherein a portion of the second conductive layer not having the position of laser spot corresponds to the first conductive layer; and

"wherein each fuse structure has one position of laser spot on the second conductive layer, and the fuse structures are insulated from one another".

Kokubun discloses a fuse structure having a first level interconnection and a second level interconnection isolated by an inter-layer insulator. The objectives of Kokubun (preventing erosion due to moisture permeation, reducing parasitic capacitance, etc.) are quite different from those of the present application (preventing the adjoining fuse structure from being damaged in the laser blow process). Naturally, the structure of the device in Kokubun is also quite different from that of the present application.

As shown in Figs. 9A and 9B, Kokubun teaches an array of a fuse structure. A first level interconnection 2 is formed on an insulating substrate 1. An insulating layer 3 is formed on the substrate 1 to cover the first level interconnection 2. A second level interconnection 4 is formed on part of the insulating layer 3 and electrically connects to the first level interconnection 2 by means of a plug 5. Two extra metal interconnections 6 extend over the insulating layer 3. It should be noted that the extra metal interconnections 6 extend parallel to the second level interconnection 4, different from a straight line arranged by the second conductive layer (340) and the third conductive layer (350) as recited by claims 1 and 9 of the present application.. Moreover, the first level interconnection 2 is not directly under the extra metal interconnections 6, unlike from the first

conductive layer (320) is directly under the third conductive layer (350), as recited by claims 1 and 9 of the present application. Also, it differs from the first conductive layer (520) is directly under the second conductive layer (540) having no laser spot (510), as recited by claims 15 and 22 of the present application.

Kokubun does not disclose the first conductive layer (320/520) directly under the third conductive layer (350) or the second conductive layer (540) having no laser spot (510), thereby protecting the first conductive layer (320/520) from damage during a laser blow process (490/690). That is, there is no disclosure of the third conductive layer (350) serving as a floating layer to directly protect the under layer (320) from laser blow damage. Also, there is no disclosure of the second conductive layer (540) having no laser spot (510) to directly protect the under layer (520) from laser blow damage. Thus, the cited reference cannot prevent both misalignment of the laser beam and thermal scattering of the laser beam from damaging the first layer (320/520) of the fuse structure in the laser blow process. The intended objective of the present application cannot be achieved by the fuse structure in Kokubun.

Niwa discloses a semiconductor device having a fuse and is used for replacement of a redundant cell. Obviously, the objective of Niwa (to replace the defective bit cell with the redundant bit cell) is very different from that of the present application (preventing the adjoining fuse structure from being damaged in the laser blow process). As a result, the structure of the device in Niwa is also quite different from that of the present application.

As shown in Figs. 3A of Niwa, a lower interconnection 302 is formed on an insulating substrate 301. An interlevel insulating film 303 is formed over the substrate 301 to cover the lower interconnection 302. An upper interconnection 305 is formed on the interlevel insulating film 303 and electrically connects to the lower interconnection 302 by means of a plug 304. An assembly pad 311 is formed on part of the interlevel insulating film 303. Nevertheless, the assembly pad 311 is not directly above the lower interconnection 302. Thus, the assembly pad 311 cannot protect the lower interconnection 302 from laser blow damage.

Niwa does not disclose the first conductive layer (320/520) directly under the third conductive layer (350) or the second conductive layer (540) having no laser spot (510), thereby protecting the first conductive layer (320/520) from damage during a laser blow process (490/690). That is, there is no disclosure of the third conductive layer (350) serving as a floating layer to protect the under layer (320) from laser blow damage. Also, there is no disclosure of the second conductive layer (540) having no laser spot (510) to protect the under layer (520) from laser blow damage. Thus, Niwa cannot prevent both misalignment of the laser beam and thermal scattering of the laser beam from damaging the first layer (320/520) of the fuse structure in the laser blow process. Niwa does not recognize the problems identified in the present application and Niwa's fuse structure cannot achieve the intended objective of the present application.

As shown in Figs. 1 and 2 of AAPA, a traditional fuse structure is disclosed. A first conductive layer M0 is formed on a substrate 100. A dielectric layer 120 is formed on part of the substrate 100 to cover the

first conductive layer M0. A second conductive layer M1 comprising a position of laser spot 110 is formed on part of the dielectric layer 120 and electrically connects to the layer M0 by means of a plug 130. Nevertheless, there is no metal layer serving as a floating layer to protect the under layer M0. When misalignment of the laser beam 290 or thermal scattering of the laser beam 290 occurs, the laser blow process can damage the M0 layer of the fuse structure.

AAPA does not disclose the first conductive layer (320/520) directly under the third conductive layer (350) or the second conductive layer (540) having no laser spot (510), thereby protecting the first conductive layer (320/520) from damage during a laser blow process (490/690). That is, there is no disclosure of the third conductive layer (350) serving as a floating layer to directly protect the under layer (320) from laser blow damage. Also, there is no disclosure of the second conductive layer (540) having no laser spot (510) to protect the under layer (520) from laser blow damage.

MPEP 2131 states that a "claim is anticipated only if **each and every element** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," quoting *Verdegaal Bros v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Under MPEP 2143, to establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Since the cited references do not teach the above-quoted limitations of claims 1, 9, 15 and 22, the Applicants respectfully submit that claims 1, 9, 15 and 22 should be allowed. Claims 2-8, 10-14, 16-21 and 23-26 should

also be allowed, at least by virtue of their dependency from claims 1, 9, 15 or 22.

The Applicants have attempted to address all of the issues raised by the Examiner in the Office Action as the Applicants understand them. The Applicants believe that the Application is now in condition for allowance. If any point requires further explanation, the Examiner is invited to telephone Troy Cai at (323) 934-2300 or e-mail Troy Cai at tcai@ladasparry.com.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account No. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

Enclosed please find a copy of Troy Guangyu Cai's Notice of Limited Recognition under 35 CFR 10.9(b) to prepare and prosecute patent applications wherein the patent applicant is a client of Ladas & Parry, and the attorney of record in the applications is a registered practitioner who is a member of Ladas & Parry.

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Expires: November 19, 2003

Harry I. Moatz
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